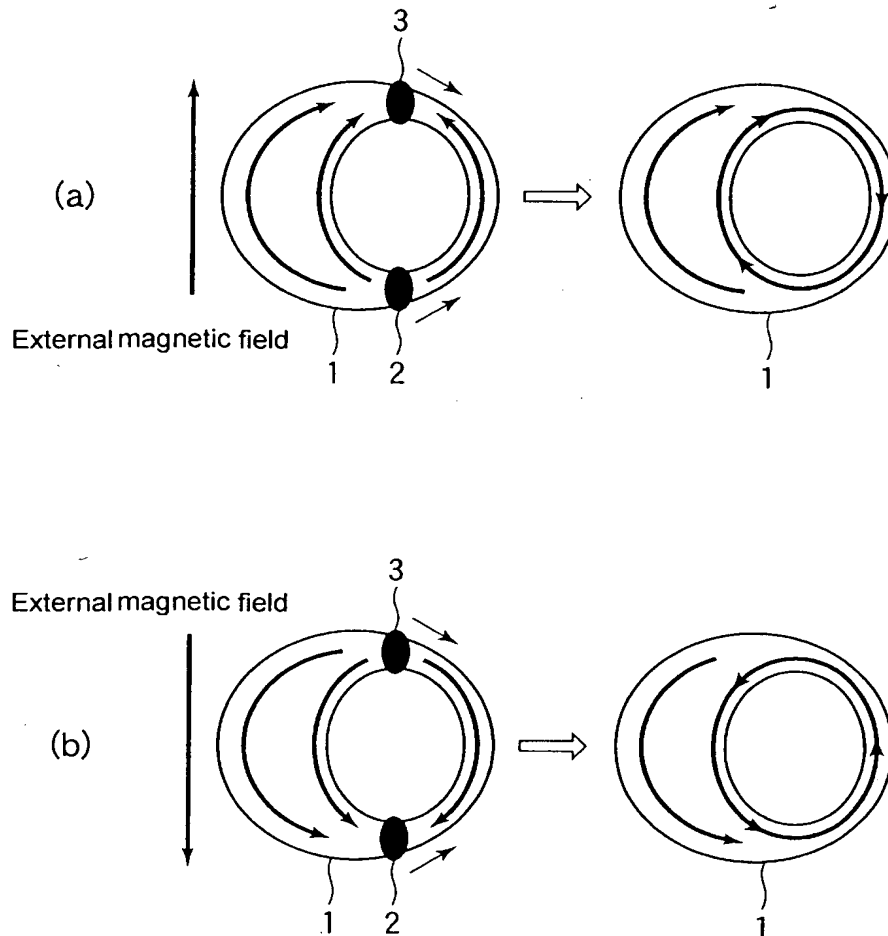


FIG. 1

Diagrams describing the configuration
according to the principles of the present invention



1: Magnetic ring 2: Magnetic domain wall 3: Magnetic domain wall

FIG. 2

Views describing the steps halfway through the manufacturing of a magnetic ring unit according to the first embodiment of the present

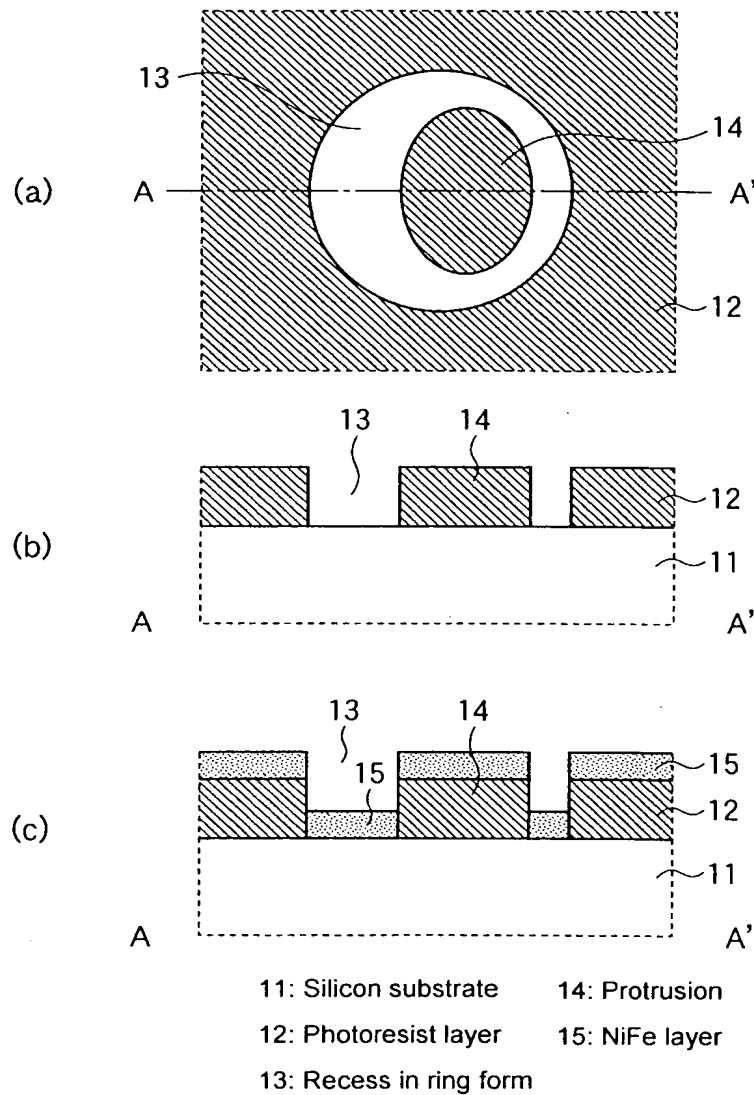
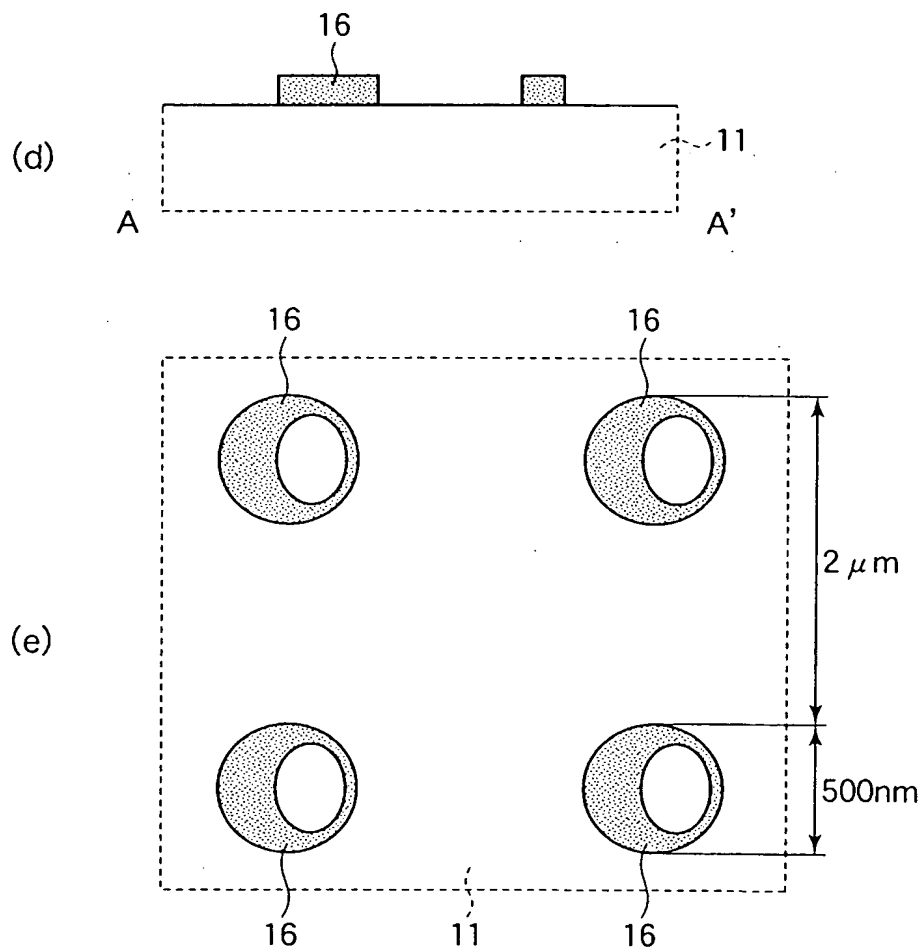


FIG. 3

Views describing the steps following Fig 2(c) of the
manufacturing of the magnetic ring unit
according to the first embodiment of the present invention

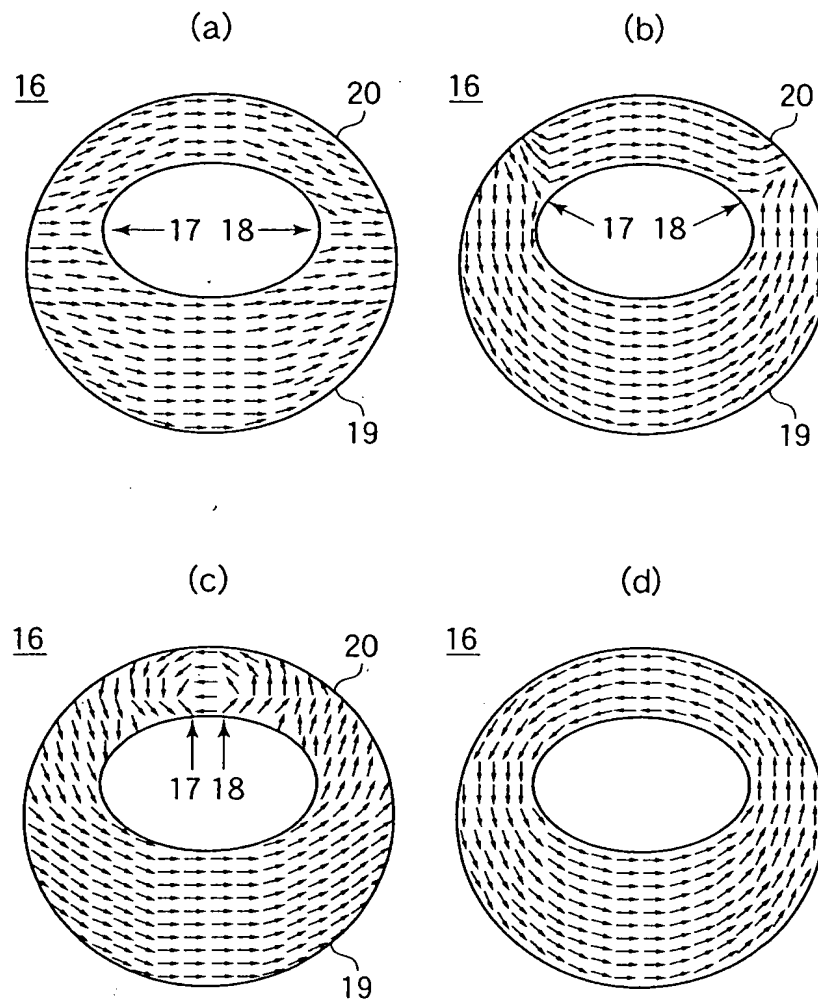


11: Silicon substrate

16: Magnetic ring unit

FIG. 4

Diagrams describing the principles of control of the direction of rotation of the magnetic moment in the magnetic ring unit according to the first embodiment of the present invention



16: Magnetic ring unit

17: Magnetic domain wall

18: Magnetic domain wall

19: Domain with broad ring width

20: Domain with narrow ring width

FIG. 5

Graph describing the hysteresis characteristics of the magnetic ring unit according to the first embodiment of the present invention

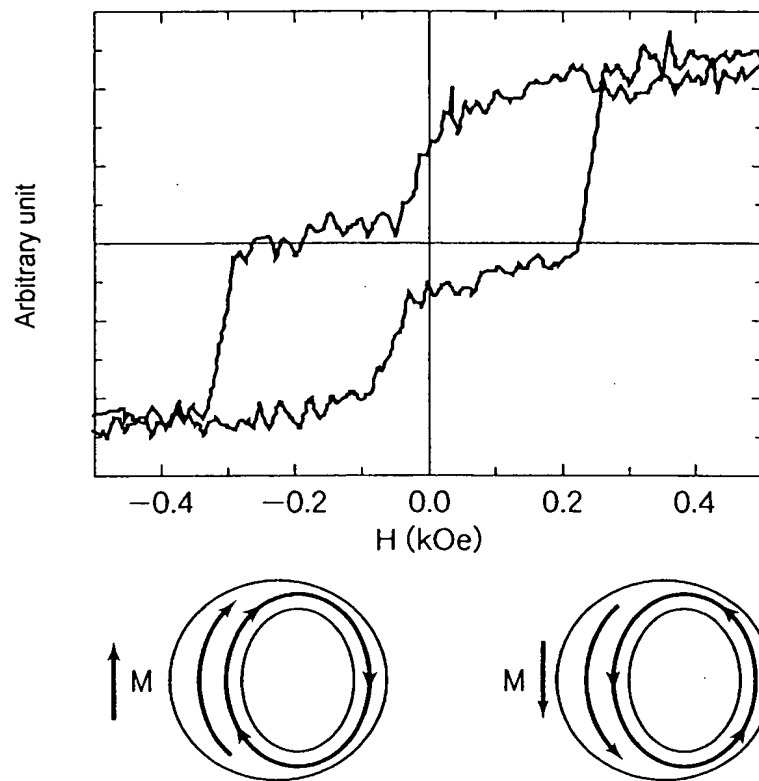


FIG. 6

Graph describing the hysteresis characteristics of a non-eccentric magnetic ring unit according to the prior art

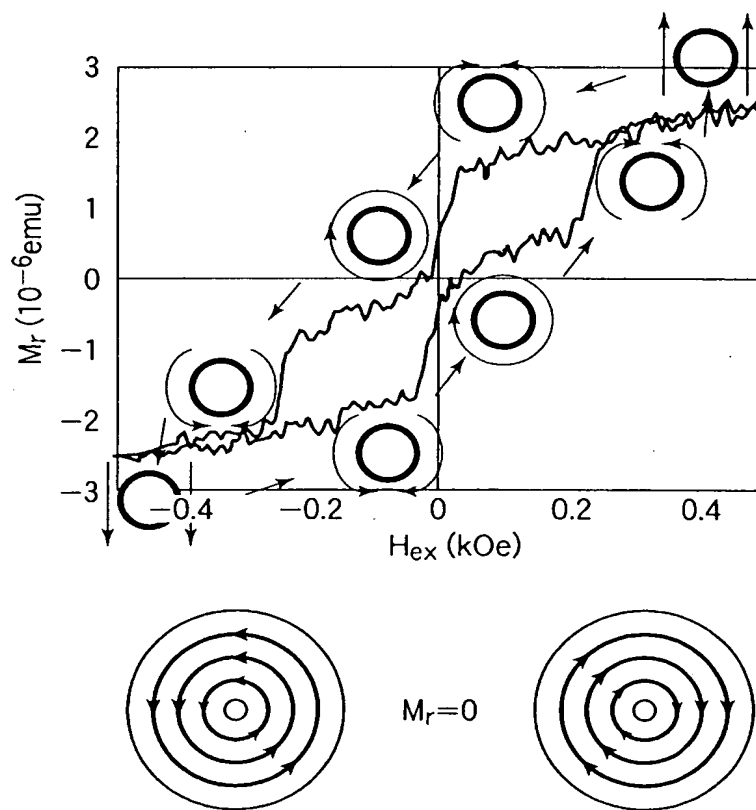
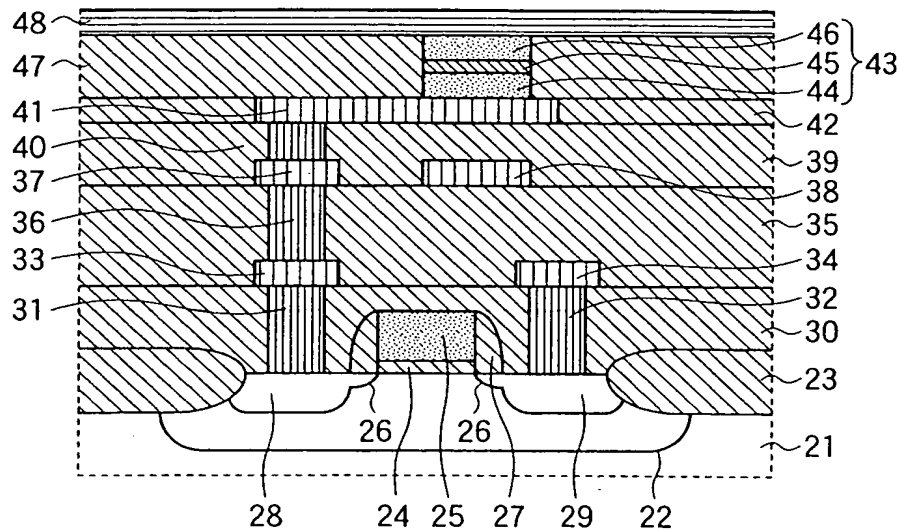


FIG. 7

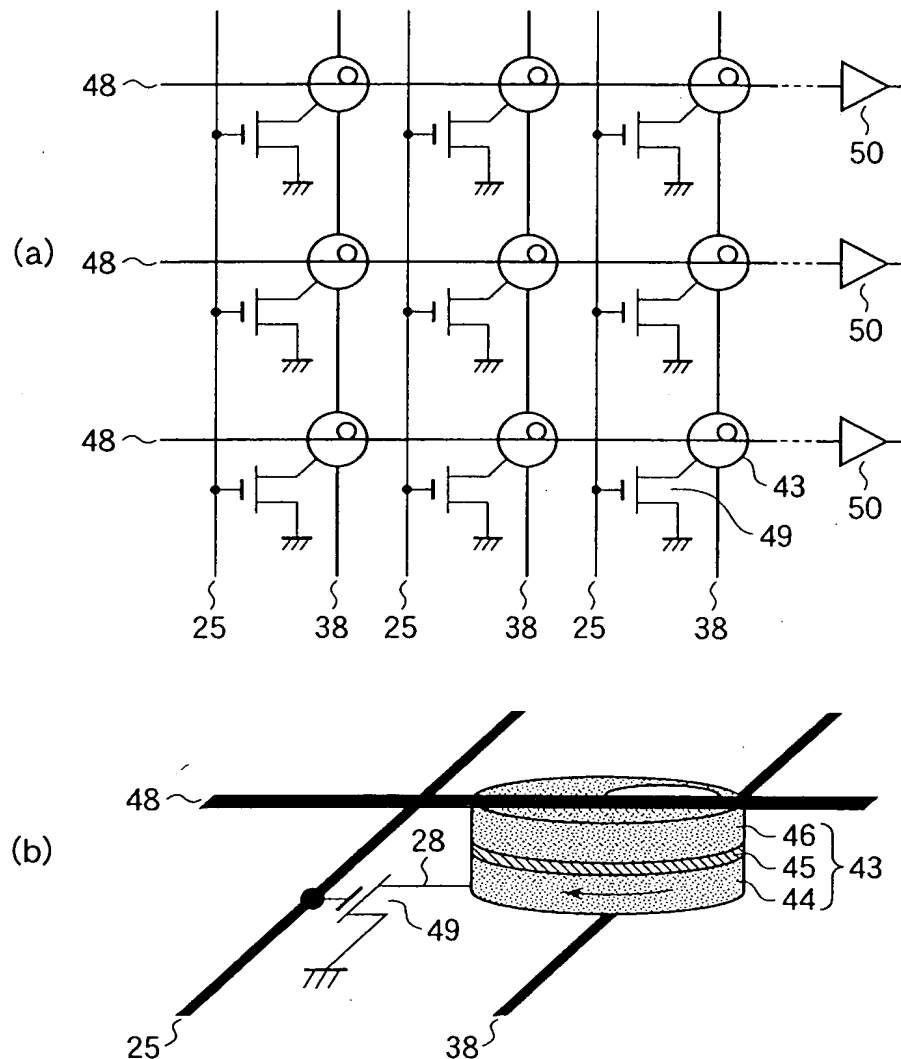
Schematic cross-sectional view showing a main portion of an MRAM according to the second embodiment of the present invention



- | | |
|--|---------------------------------------|
| 21: n-type silicon substrate | 35: Second interlayer insulating film |
| 22: p-type well region | 36: W plug |
| 23: Element isolation oxide film | 37: Connecting conductor |
| 24: Gate insulating film | 38: Word line |
| 25: Sense line | 39: Third interlayer insulating film |
| 26: n ⁻ -type LDD region | 40: W plug |
| 27: Sidewall | 41: Lower electrode |
| 28: n ⁺ -type drain region | 42: Fourth interlayer insulating film |
| 29: n ⁺ -type source region | 43: Magnetic ring unit |
| 30: First interlayer insulating film | 44: NiFe layer |
| 31: W plug | 45: Tunnel insulating film |
| 32: W plug | 46: CoFe layer |
| 33: Connecting conductor | 47: Fifth interlayer insulating film |
| 34: Ground line | 48: Bit line |

FIG. 8

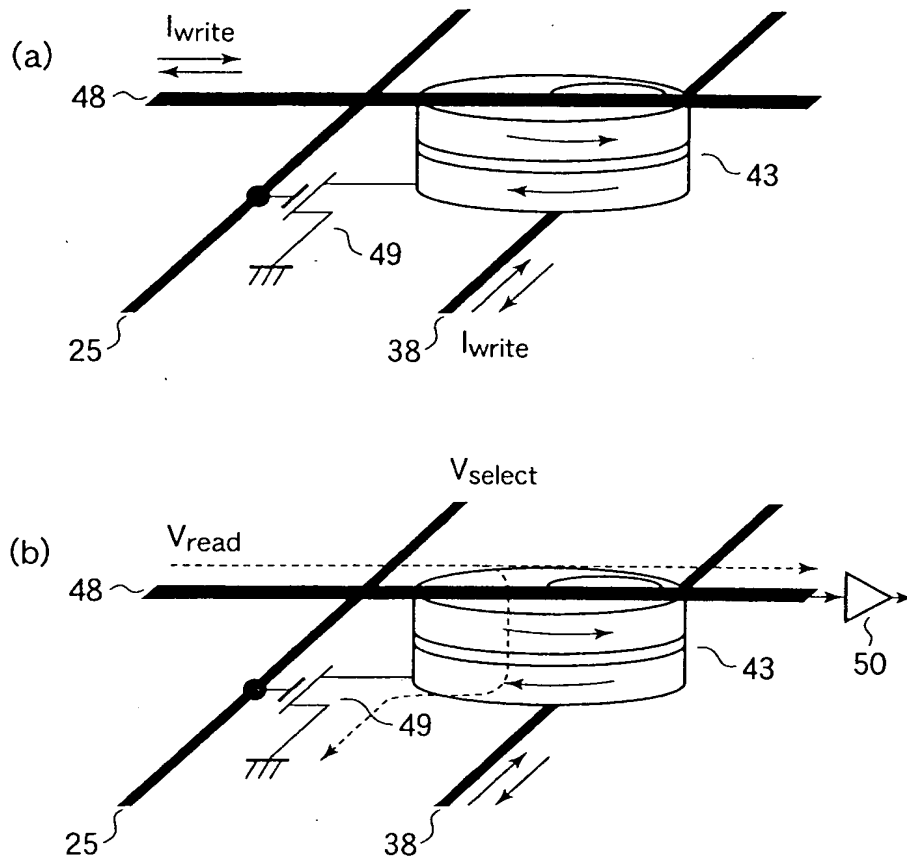
Diagrams describing the circuit configuration of the MRAM according to the second embodiment of the present invention



- | | |
|---------------------------------------|----------------------------|
| 25: Sense line | 45: Tunnel insulating film |
| 28: n ⁺ -type drain region | 46: CoFe layer |
| 38: Word line | 48: Bit line |
| 43: Magnetic ring unit | 49: Access transistor |
| 44: NiFe layer | 50: Sense amplifier |

FIG. 9

Diagrams describing write-in and read-out operations in the MRAM according to the second embodiment of the present invention



25: Sense line	48: Bit line
38: Word line	49: Access transistor
43: Magnetic ring unit	50: Sense amplifier

FIG. 10

Diagram showing a conceptual configuration of magnetic moment distribution in a nanoring unit

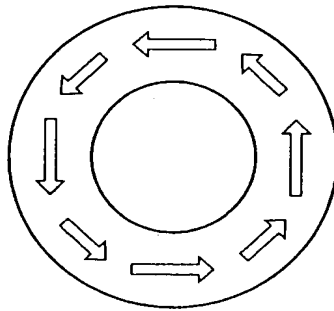


FIG. 11

Diagrams describing the conversion from the opposed domain structure to the magnetic vortex structure in the nanoring unit

